REMARKS

Applicants have studied the Office Action dated March 29, 2004 and have made amendments to the claims. It is submitted that the application, as amended, is in condition for allowance. By virtue of this amendment, claims 7, 9-23, 33, 34, and 37 are pending. Claims 1-6, 8, 30-32, 35, 36, and 38 have been canceled without prejudice. Claims 7, 11, 14, 16, 17, 19, 21, 22, and 37 have been amended. Reconsideration and allowance of the pending claims in view of the above amendments and the following remarks are respectfully requested.

The drawings were objected to under 37 C.F.R. § 1.83 as failing to show every feature of the invention specified in the claims. Applicants have canceled all claims that recited the feature that was objected to by the Examiner. Thus, this objection is moot.

Claims 35, 36, and 38 were rejected under 35 U.S.C. § 112, first paragraph. Claims 35, 36, and 38 have been canceled so this rejection is moot.

Claims 1, 2, 4-6, and 30-32 were rejected under 35 U.S.C. § 102(e) as being anticipated by Deboer et al. (U.S. Patent No. 6,677,636). Claims 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Deboer et al. in view of Maeda (U.S. Patent No. 6,358,820). Claims 1-6 and 30-32 have been canceled so these rejections are moot.

Claims 7-23, 33, 34, and 37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Deboer et al. in view of Abernathey et al. (U.S. Patent No. 5, 453,400). Claims 10 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Deboer et al. in view of Maeda (U.S. Patent No. 6,358,820). Claim 8 has been canceled so, with respect to this claim, these rejections are moot. With respect to claims 7, 9-23, 33, 34, and 37, these rejections are respectfully traversed.

The present invention is directed to providing easy to manufacture electrical contacts having low-resistance for an integrated circuit that has a passive component above active components. One embodiment provides an integrated circuit that has transistors, passive components, and a level of local metal connections formed within a first insulating layer that is deposited on top of the transistors. The integrated circuit includes first, second, and third metal terminals that each consist of a single layer of metal formed within a cavity passing completely through the thickness of the first insulating layer such that the metal terminal passes completely through the thickness of the first insulating layer.

The first metal terminal constitutes a first stage of contact between one active area of the integrated circuit and a first level of interconnection, has a lower surface that contacts the one active area of the integrated circuit, and has an upper surface that contacts a second stage of contact between the one active area of the integrated circuit and the first level of interconnection. The second metal terminal vertically connects one active area of the integrated circuit to a passive component that directly contacts the upper surface of the first insulating layer, and the third metal terminal horizontally connects two separate active areas of the integrated circuit. Additionally, the second metal terminal has a lower surface that contacts a junction of one of the transistors of the integrated circuit such that the lower surface of the second metal terminal extends over a boundary of the junction of the one transistor.

Because the three metal terminals each consist of a single layer of metal formed within a cavity passing completely through the thickness of the insulating layer such that the metal terminal passes completely through the thickness of the insulating layer, all three terminals can be easily manufactured in a simultaneous manner while providing low electrical resistance.

The Deboer reference discloses a method of forming a bit line contact during DRAM fabrication in which an intermediate plug is formed to reduce the contact aspect ratio. The Abernathey reference discloses methods for interconnecting polysilicon zones on a semiconductor substrate. However, neither Deboer nor Abernathey, or a combination of the two, discloses an integrated circuit that includes a first metal terminal that constitutes a first stage of contact between one active area of the integrated circuit and a first level of interconnection, a

second metal terminal that vertically connects one active area of the integrated circuit to a passive component that directly contacts the upper surface of the first insulating layer, and a third metal terminal that horizontally connects two separate active areas of the integrated circuit, with the first, second, and third metal terminals each consisting of a single layer of metal formed within a cavity passing completely through the thickness of the first insulating layer such that the metal terminal passes completely through the thickness of the first insulating layer, as is recited in amended claim 7. Amended claims 14 and 19 contain similar recitations.

As recognized by the Examiner, the Deboer reference fails to disclose a metal terminal horizontally connecting two active areas of the integrated circuit and consisting of a single layer of metal that passes completely through the thickness of the first insulating layer (i.e., the third metal terminal). However, the Examiner went on to state that the Abernathey reference makes up for this deficiency in the disclosure of Deboer by disclosing such a metal terminal. This position of the Examiner is respectfully traversed.

Abernathey is directed to interconnecting polysilicon zones on a semiconductor substrate. In one method, Abernathey teaches selectively growing a tungsten layer 34 over a polysilicon layer 26 so as to connect two doped source/drain regions 12 that are separated by a recessed oxide region 14, as shown in Figure 2B. In another method, Abernathey teaches depositing a tungsten layer 34 over the entire substrate and then heating the structure to form a titanium silicide layer 38 where the titanium was in contact with a polysilicon layer 26. The titanium that was not formed into silicide is removed so as to leave only the titanium silicide layer 38 that connects two doped source/drain regions 12 that are separated by a recessed oxide region 14, as shown in Figure 3D.

Thus, while Abernathey does teach a metal layer that connects two active areas of an integrated circuit, this metal layer is simply formed over the existing circuit elements. In other words, Abernathey does not teach connecting the two active areas using a metal terminal that is formed within a cavity that passes completely through the thickness of an insulating layer that

overlies the transistors of the integrated circuit, such that the metal terminal passes completely through the thickness of the insulating layer.

In contrast, preferred embodiments of the present invention provide an integrated circuit having first, second, and third metal terminals that pass completely through the thickness of an insulating layer that overlies the transistors of the integrated circuit. The first metal terminal constitutes a first stage of contact between one active area of the integrated circuit and a first level of interconnection, and the second metal terminal vertically connects one active area of the integrated circuit to a passive component that directly contacts the upper surface of the insulating layer. The third metal terminal horizontally connects two separate active areas of the integrated circuit. Further, each of these three metal terminals consists of a single layer of metal formed within a cavity passing completely through the thickness of the insulating layer such that the metal terminal passes completely through the thickness of the insulating layer.

Thus, in preferred embodiments of the present invention, two active areas of the integrated circuit are horizontally connected by a metal terminal that is formed within a cavity that passes completely through the thickness of the insulating layer that overlies the transistors of the integrated circuit, such that the metal terminal passes completely through the thickness of the insulating layer. Such a metal terminal formed within a cavity that has been previously formed so as to pass completely through the thickness of an insulating layer is completely different than connecting two active areas of the integrated circuit by a metal layer that is formed over the existing circuit elements. Because the three metal terminals metal terminal are formed within cavities that pass completely through the thickness of the insulating layer that overlies the transistors of the integrated circuit, all three terminals can be easily manufactured in a simultaneous manner while providing low electrical resistance.

Furthermore, Applicants submit that it is improper to combine the Deboer and Abernathey references because, even if each of Deboer and Abernathey suggest one of the recited terminals of the claimed integrated circuit, there is no teaching or suggestion to simultaneously use three such metal terminals in a single insulating layer of a device. The Examiner has not

cited any reference or generally available knowledge that suggests or provides any motivation for combining the general feature of an overlying metal layer connecting two active regions that is disclosed in Abernathey with the DRAM structure disclosed in Deboer so as to produce a plug structure that passes completely through the thickness of an insulating layer that overlies the transistors of an integrated circuit in combination with two other metal terminals that pass completely through the thickness of the insulating layer as is recited.

Nearly all integrated circuit structures include the same basic elements and features (such as conducting lines and regions, insulating layers and regions, semiconductor regions, doped regions, an contacts) combined in different manners with very different results. If all that was required to sustain a finding of obviousness was that each separate feature of an integrated circuit structure was disclosed in some other integrated circuit structure, then few (if any) integrated circuit structure patents would be issuing at this time. However, a great number of such patents continue to issue because this is certainly not the law and there must be shown some specific motivation for combining a feature found in one reference in a specific manner into a different type of circuit structure found in another reference in order to sustain a finding of obviousness.

Here, the specific structure and arrangement of the three metal terminals in the first insulating layer makes it possible to realize all the necessary connections within the first insulating layer in a simultaneous manner while providing low electrical resistance. Besides providing easy to manufacture and low resistance contacts, all of the interconnections in the first insulating layer are formed at the beginning of the manufacturing process.

Additionally, Applicants submit that it is not possible to simply insert the overlying metal layer connecting two active regions of Abernathey into the very different DRAM structure of Deboer. Such an overlying layer could not feasibly be formed within the DRAM structure of Deboer along with the other two terminals so as to form three terminals within cavities passing completely through the thickness of the insulating layer such that the metal terminals pass completely through the thickness of the insulating layer. Thus, the combination of Deboer and Abernathey suggested by the Examiner is unworkable. At the least, neither reference provides any motivation for combining such features into one integrated circuit, or teaches how such features can be combined to create the recited structure.

The cited references fail to meet the basic requirement for a finding of obviousness established by the courts. There is simply no suggestion or motivation in any of these references for combining selected features of one reference with the integrated circuit structure of the other reference in order to produce a single integrated circuit structure, nor is there any suggestion of the desirability of such a combination. Without Applicants' specification, there would be no suggestion or motivation to one of ordinary skill in the art at the time of the invention to produce the recited structure. It is respectfully submitted that the Examiner is engaging in hindsight reconstruction of the claimed invention.

Neither Deboer nor Abernathey, or a combination of the two, teaches or suggests an integrated circuit that includes a metal terminal horizontally connecting two separate active areas of the integrated circuit, with the metal terminal consisting of a single layer of metal formed within a cavity passing completely through the thickness of an insulating layer that overlies the transistors of the integrated circuit, such that the metal terminal passes completely through the thickness of the first insulating layer.

Applicants believe that the differences between Deboer, Abernathey, and the present invention are clear in amended claims 7, 14, and 19, which set forth various embodiments of the present invention. Therefore, claims 7, 14, and 19 distinguish over the Deboer and Abernathey references, and the rejection of these claims under 35 U.S.C. § 103(a) should be withdrawn.

As discussed above, claims 7, 14, and 19 distinguish over the Deboer and Abernathey references. Furthermore, the claimed features of the present invention are not realized even if the teachings of Maeda are incorporated into Deboer and Abernathey. Maeda does not teach or suggest the claimed features of the present invention that are absent from Deboer and Abernathey. Thus, claims 7, 14, and 19 distinguish over the Deboer, Abernathey, and Maeda references, and thus, claims 9-13, 33, 34, and 37, claims 15-18, and claims 20-23 (which depend from claims 7, 14, and 19, respectively) also distinguish over the Deboer, Abernathey, and

Maeda references. Therefore, it is respectfully submitted that the rejections of claims 7, 9-23, 33, 34, and 37 under 35 U.S.C. § 103(a) should be withdrawn.

In view of the foregoing, it is respectfully submitted that the application and the claims are in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is invited to call the undersigned attorney at (561) 989-9811 should the Examiner believe a telephone interview would advance the prosecution of the application.

Respectfully submitted,

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